M&N-IT-557

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applic. No.	:	10/649,602 Confirmation No. 5514
Applicant	:	Karl Schrödinger
Filed	:	August 27, 2003
Title	:	Optical Receiver Circuit
Group Art Unit	:	2613
Examiner	:	Luis F. Garcia
Docket No.	:	M&N-IT-557
Customer No.	:	24131

DECLARATION UNDER 37 C.F.R. § 1.131

I, Karl Schrödinger, sole inventor of the invention described and claimed in the instant application hereby declare that:

The invention was "reduced to practice" in Germany, a WTO member country, at least as early as October 18, 2002.

Enclosed, as corroborating evidence is a document listing me as the patent engineer (i.e., "Bearb. Schrödinger"), dated (i.e., "datum") October 18, 2002, and entitled "Preliminary Specification Receiver IC for Plastic Fiber Applications".

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Karl Schrödinger _____ Date _____

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Preliminary Specification

50 Mb/s Optical Receiver IC for Plastic Optical Fiber (POF) Applications

APPLICATIONS:

- POF systems up to 50Mbit/s
- MOST systems

FEATURES:

- Integrated *Light to Logic Receiver* with power down functionality
- Data rate up to 50 MBd
- Supply voltage range from 3.135V to 3.465V and 4.75V to 5.25V
- LVCMOS data output and status signal (signal detect)
- All functions realized in 0.5µm mixed signal CMOS technology

TECHNOLOGY:

- CMOS C5NA
- FC-Number: V23481-S1-A69
- Chip-Number: M13B4A11

RELATED DOCUMENTS:

- [1] MOST Specification of Physical Layer, Ver. 1.0
- [2] BIGFOOT Datasheet, OS 8300, 22.03.2001
- [3] Infineon Data sheet SFF MOT 003, 21.06.2001

signed: Thomas Lichtenegger : Harald Dopke :

Changes:

Rev.	Changes	Pages
51	Initial Version	
52	photodiode model, layout, characteristics,	6, 9-13
53		

				Datum	18 10 02	Preliminary Specification Receiver IC for Plastic Fiber Applications M1384	
				Bearb.	Schrödinger		
				Gepr.			
				Norm			
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52		0411 02	scr	Infineon Technologies		W23481-S1-A69-*-59 Company Confidential	1/13
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GENERAL DESCRIPTION

Fig. 1 shows the block diagramm of the receiver chip.

Receiver Functionality

The receiver consists of the following circuit blocks:

- Differential transimpedanceamplifier (TIA)
- Differential post amplifier (PA)
- Single ended CMOS output driver
- Current sense, network activity detection and power down circuit
- Signal detect
- Voltage regulator

The *TIA* consists of a differential or two single ended CMOS TIAs. Therefore for differential use a 2nd input is available (inverted, may be left open for single ended usage). If this inputs (IN, INn) are used differentially with a differential photo diode an improved PSSR is guaranteed. On the TIA input (IN) a DC control current is applied to hold the input free from DC current and so the output of both TIAs have zero offset voltage (see detailed block diagram in fig. 2). A peak detect and an amplitude control circuit is implemented to control the TIA feed back resistance for a high dynamic range. A low pass filter on the kathode of the photodiode is implemented for improving PSRR (bandwidth of low pass tbd.).

The postamplifier amplifies the TIA output signal to the necessary level for the CMOS output driver.

The output driver may have a *Duty Cycle Control* function (optional). The duty cycle is regulated to zero at a voltage level of 1.5V. The driver has to drive a load capacitance of 10pF.

Power Down Mode Circuit and Network Activity Detection

The circuit contains a power down functionality. This circuit is used to power down the chip if the optical data input is at a level smaller than -40dBm for longer than 8.5 µs. The SD output becomes high and data output low if the chip is in low power mode. A low power comparator remains powered up during low power mode and monitors the photodiode current.

For waking up a timer and a network activity detector is used to put the part out of low power mode if the power rises above -25dBm. Once current is detected by the current monitor, the IC checks for any network activity before it powers up fully.

The network activity check is done after power up in 2 steps as described as follows.

As 1st step, if the current sensor has recognized a current above the threshold, a low power oscillator is starting and monitors the photo diode current after 345µs again. If there is still power above the threshold recognized, the network activity check is continued and the receiver is powered up totally. If not, the oscillator is powered down.

In the 2nd step of power up, a data detector looks to the data output of the receiver for 27µs. If the number of data edges is lower than 12 or higher than 1536, the chip will go in low power mode again and switch off the power. Otherwise the chip will enter into the final full operating mode.
The SD output becomes low and the data output has valid data after reaching the final operating mode.
Fig. 3 shows the state diagram of the sleep mode and network activity sense.

Furthermore the circuit contains a voltage regulator to insure operation at 3.3 and 5V.

Test Mode

No Test Mode planned for now.

Test Circuit

Fig. 4 shows the test circuit for the receiver. If noise signal is applied (u_n), the blocking capacitor CP must be removed. Output signal is measured with a high impedance probe and 10pF load capacitance.

Photo Diode Model

Fig. 5 shows the model of the differential photo diode. The values are defined in the specification in last chapter. The fig. 6 shows the reference signal pulse form to be used for simulations (out of [1]).

FIGURE 1: GENERAL CIRCUIT BLOCK DIAGRAMM

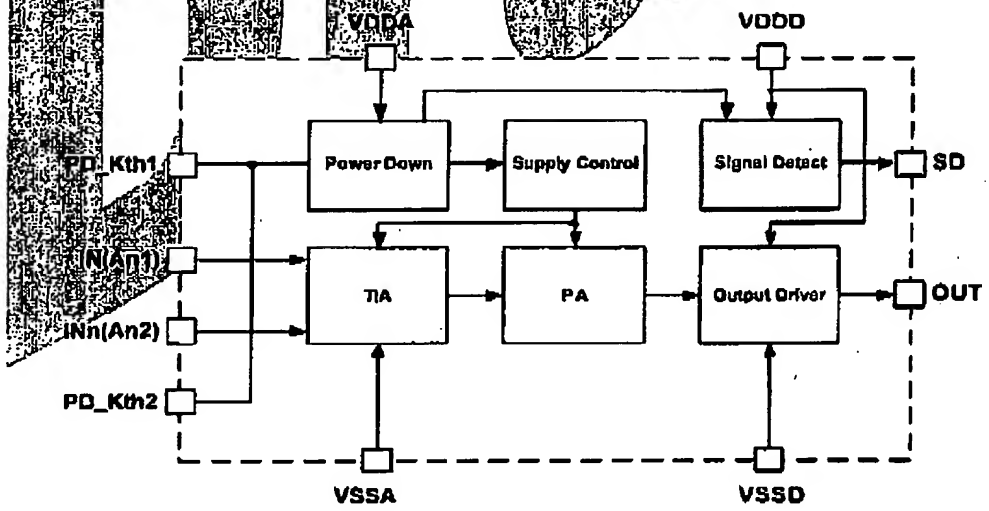
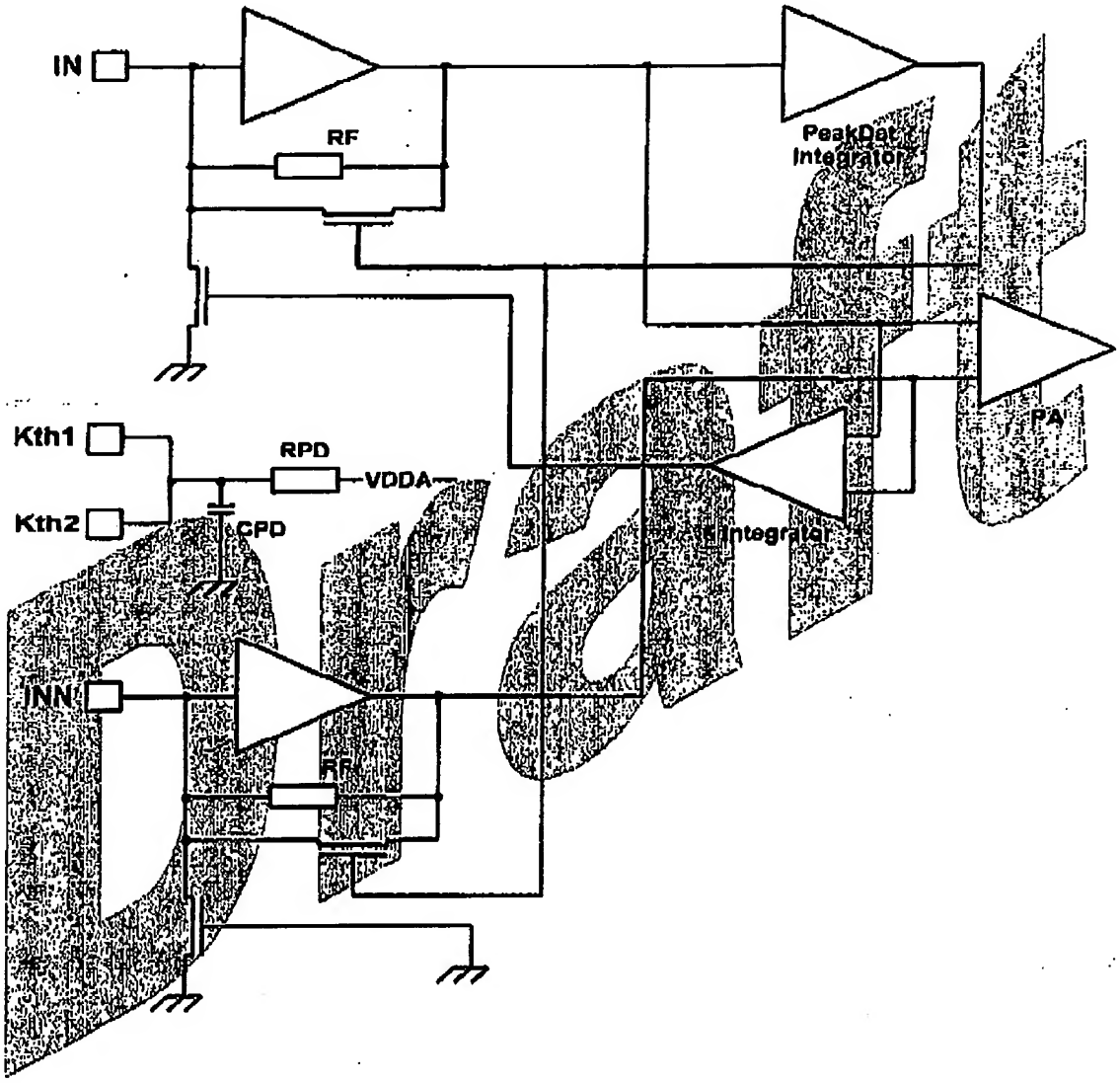


FIGURE 2: DETAILED TIA BLOCK DIAGRAM



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51		18 10 02	scr				
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FIGURE 3: STATE DIAGRAMM FOR SLEEP MODE AND NETWORK ACTIVITY SENSE:

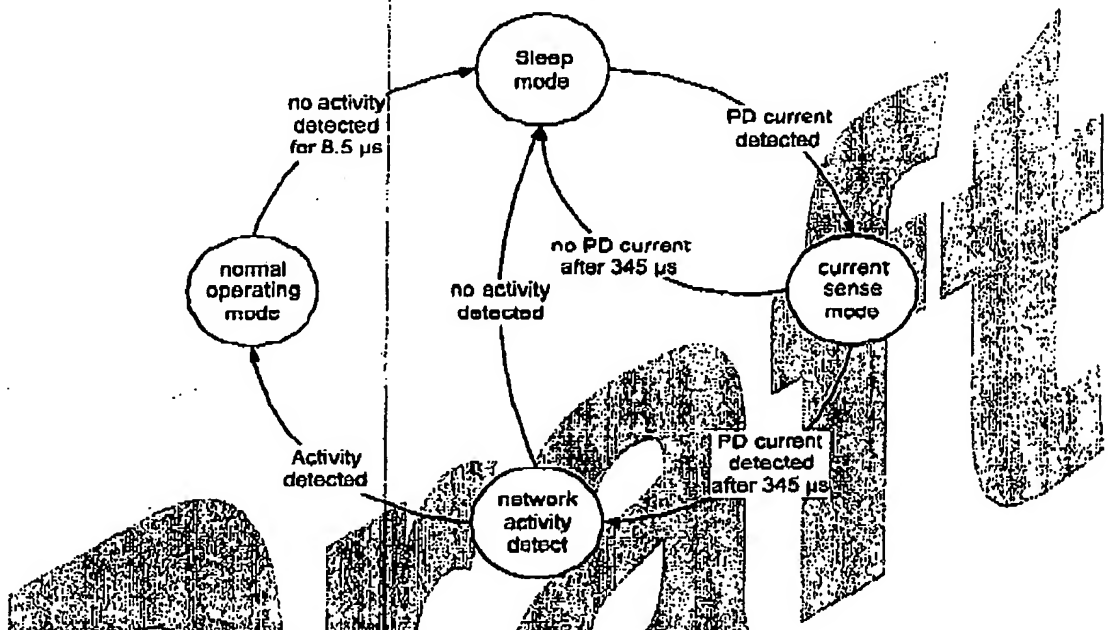
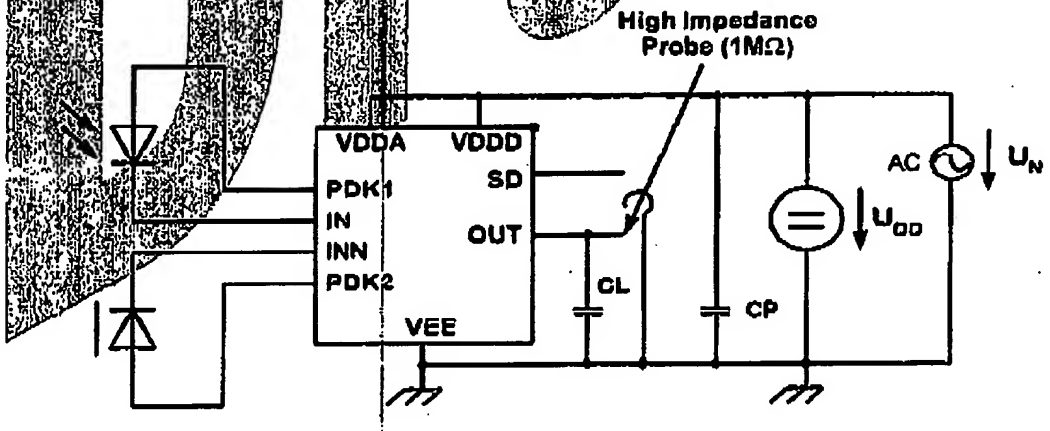


FIGURE 4 : TEST CIRCUIT FOR THE RECEIVER CIRCUIT
(OUT and SD to be tested with high impedance scope probe. CP to be removed for PSRR testing.)



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51		18 10 02	scr				
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FIGURE 5: DIFFERENTIAL PHOTODIODE MODEL

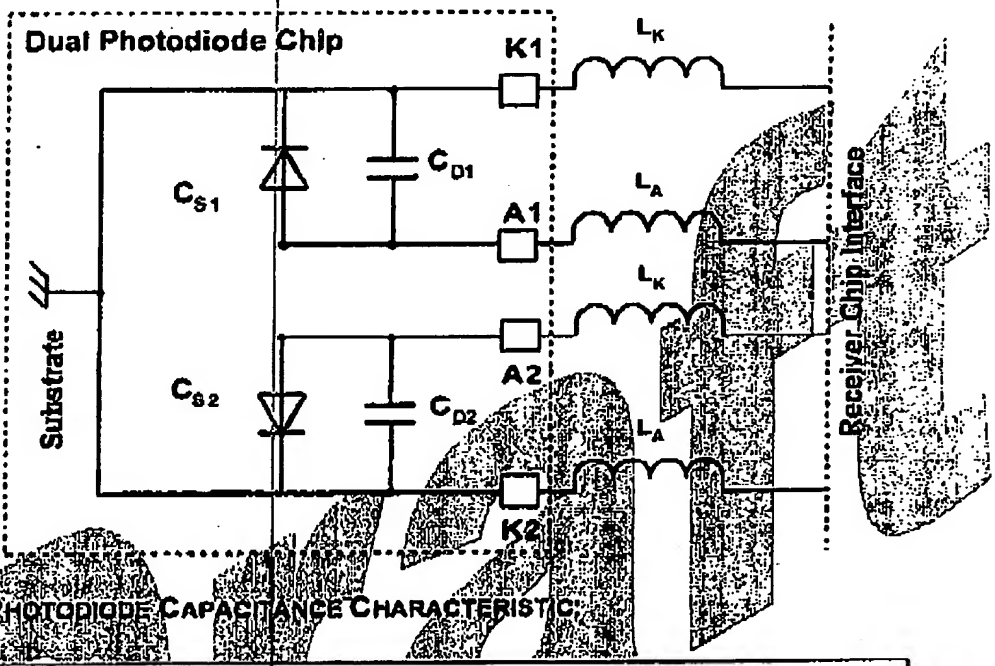
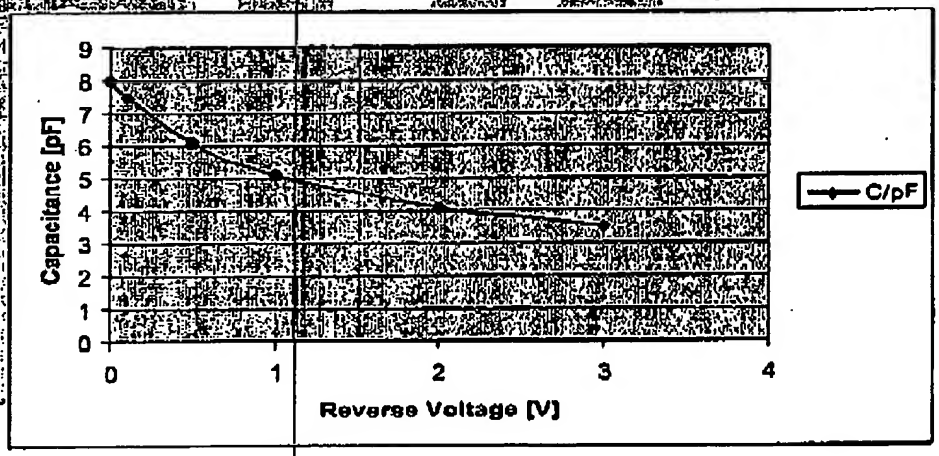


FIGURE 6: PHOTODIODE CAPACITANCE CHARACTERISTIC



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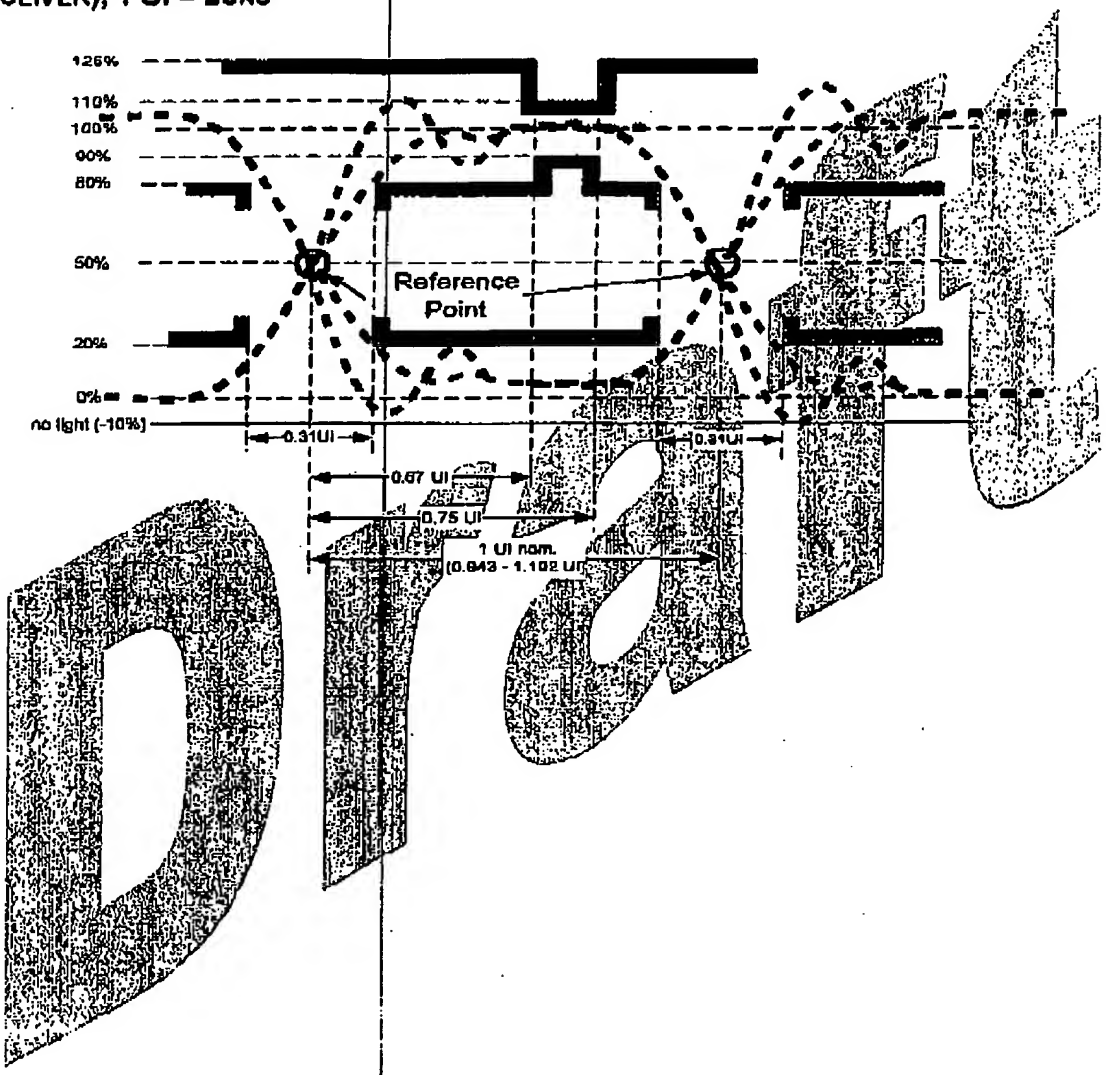
52		0411 02	scr				
51		18 10 02	scr				
Zust.	Mitteilung	Datum	Name			Data: M1304_Spec52_MOST_Rx	

FIGURE 7 : MOST OPTICAL PULSE CHARACTIERISTIC (INPUT CURRENT SIGNAL OF RECEIVER), 1 UI = 20NS



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				Gepr.			
				Norm			
				COM FO E IC			
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51		18 10 02	scr				
Zust.	Mitteilung	Datum	Name			Datei: M1384_6pac52_MOST_Rx	

Absolute Maximum Ratings

Absolute Maximum Ratings may not be exceeded without causing permanent damage or degradation. Exposure to these values for extended periods may effect device reliability. If the device is operated beyond the range of Operating Conditions and Characteristics functionality is not guaranteed. All voltages given within this data sheet are referred to Vss if not otherwise mentioned.

Rating	Unit	Min	Max	Note
Supply Voltage V_{DD}-V_{SS}	V	-0.5	8	
Power dissipation P_{tot}	mW		300	
Voltage at at any PIN	V	-0.5	V_{DD}+0.5	
DC current at any PIN except power	mA	-10	10	
Storage temperature	°C	-65	150	
Processing temperature 1	°C		260	For 10 sec
Processing temperature 2	°C		180	For 6 h
Electrostatic Discharge Voltage Capability	kV		2	1
Electrostatic Discharge Voltage Capability	V		500	2
Electrostatic Discharge Voltage Capability	V		200	3

1 ESD Capability for all Pins except IN, INN, acc. HBM MIL-Std. 883D (human body model)
2 ESD Capability for Input Pins IN, INN, acc. HBM MIL Std. 883D (human body model)
3 ESD Capability for all Pins except IN, INN, acc. Machine model

General Operating Conditions

Under the below defined operating conditions all specified characteristics will be met unless otherwise noted. All voltages are referenced to V_{SS} unless otherwise noted.

Operating Condition	Unit	Min	Max	Note
Environmental				
Junction Temperature	°C	-40	125	
Supply Voltage high V_{DD}	V	4,75	5,25	
Supply Voltage low V_{DD}	V	3,135	3,465	

Electrical Characteristics

SP	Characteristics / Operating Conditions	Symbol	Unit	Min	Typ	Max	Note
General DC Characteristics							
1	Supply current V_{DD} (normal mode)	I_{DD}	mA		12(18)	16(22)	4
2	Supply current V_{DD} (low power mode)	I_{DD}	µA		5	10	5
3	Output voltage low, OUT, SD	V_{OUT_LOW}	V	0		0.4	6
4	Output voltage high, OUT, SD	V_{OUT_HIGH}	V	V_{DD}		V_{DD}	7
5	Input bias voltage at IN, INN	V_{IN_BIAS}	V	0.65	0.9	1.15	8
AC Characteristics							
6	Data rate	DR	MBit/s	8		50	
7	Optical input power, for data transmission	P_{IN_DATA}	dBm	-26		-2	9
8	Optical input power for power up	$P_{IN\_P\_UP}$	dBm	-39		-26	10
9	Optical input power for power down	$P_{IN\_P\_DWN}$	dBm	-40		-26	10
10	Power supply rejection ratio	PSRR	dB		30		11
11	Optical input rise and fall time	t_{R_IN}, t_{F_IN}	ns			6.2	12

4 Normal operating mode, data transmission of 25MBit/s machester coded data, 50% duty cycle of data transmitted, C_{LOAD} = 10pF, values in brackets are current IC values
5 Low Power Mode (power down modus), no current through SD output
6 at 2.4 mA sink current
7 at 2.4 mA source current
8 no input current
9 During data transmission, the jitter specification has to be kept. I_{IN} to be calculated with 0.36A/W, extinction ratio > 10dB ; Sensitivity for a BER of 10^{-9} at eye center eye is -28 dBm.
10 Input range for power down and network activity sense functionality
11 PSRR at the output of the TIA, guaranteed by design (simulation)
12 20% to 80 %.

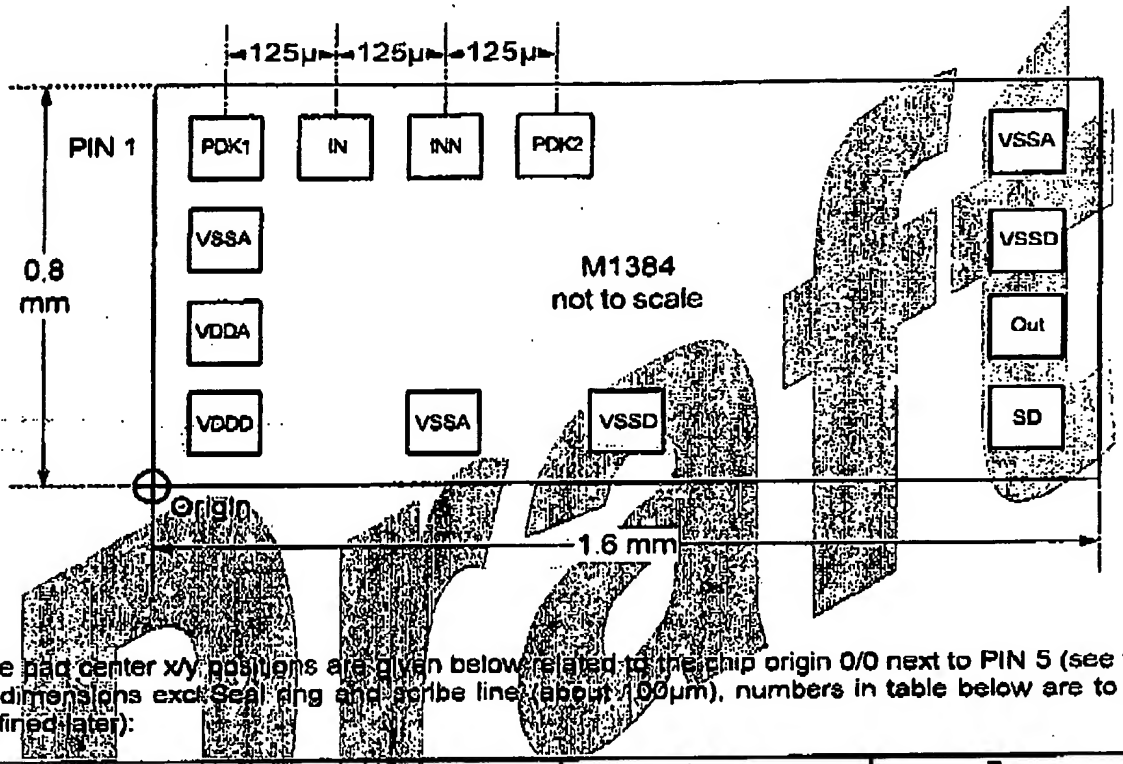
12	Pulse width variation of optical input, @ 50MBd,	t_{P_IN}	ns	18.88		22.04	13
13	Avg. Pulse width variation of optical input, @ 50MBd	$t_{P\_IN\_AVG}$	ns	-0.46		1.34	14
14	Output rise time	t_{R_OUT}	ns		7.5	9	15
15	Output fall time	t_{F_OUT}	ns		7.5	9	16
16	Output pulse width variation	t_{P_OUT}		14		29.6	17
17	Average output pulse width variation	$t_{P\_OUT\_AVG}$		0		7.2	18
18	Power up time at rising VDD	t_{PUP_VDD}	ms		2.5	15	
19	Power up time from low power mode	$t_{PUP\_L\_POW}$	ms		2.5	15	19
20	Power down time	$t_{PUP\_L\_POW}$	µs	6	10	20	
21	Delay for 2nd PD current measurement	$t_{DEL\_PD\_TST}$	µs	270	345	420	
22	Counter window for activity test	t_{WIN_ACT}	µs	20	27	33	
23	Lower cut off frequency	f_{CUT}	kHz		50	100	20
24	Low pass for photo diode kaput	f_{PD_FIL}	kHz		800	1000	21
25	Filter resistor RPD	RPD	Ω		1000		
26	Filter capacitor CPD	CPD	pF		200		
Photo Diode Characteristics							
28	Diode capacitance	C_D	pF			4	22
26	Bond-Wire Inductance	L_B	nH		1n		
27	Responsivity	R	A/W	0.36	0.4	0.44	

13 at 50 % signal amplitude acc. [1]
14 at 50 % signal amplitude acc. [1]
15 Cload = 10pF, 10% to 90 %
16 Cload = 10pF, 10% to 90 %
17 measured at -1.9V acc. [1], includes data distortion of input signal
18 measured at -1.9V acc. [1], includes data distortion of input signal
19 from receiving last data bit to shut down supply current
20 of data channl, depends on simulation results with manchester coded PRBS 2^7-1 data
21 consisting of RPD, CPD
22 @ -1.9V reverse voltage, see model fig. 5 and fig. 6.

PIN DESCRIPTION

PIN #	Signal Name	Type	Description
1	PDK1	PD cathode connection 1	Photo diode cathode connection #1 for active PD
2	V_{SSA}	Power	GND connection, preferred analog GND connection
3	V_{DDA}	Power	Positive supply voltage for analog block TIA
4	V_{DDD}	Power	Positive supply voltage for CMOS output driver
5	V_{SSA}	Power	GND connection, optional analog GND connection
6	V_{SSD}	Power	Digital GND connection
7	SD	Output	Signal detect (status) output
8	OUT	Output	Receiver data output
9	V_{SSD}	Power	Digital GND connection
10	V_{SSA}	Power	GND connection, optional analog GND connection
11	PDK2	PD cathode connection 2	Photo diode cathode connection #2 for blind PD
12	INN	PD Data Input 2	Complementary (inverted) optical input
13	IN	PD Data Input 1	Optical input, a high input current gives a high output level at OUT

FIG. 8 : PAD LAYOUT (PRELIM. PROPOSAL):
(Dimensions excl.Seal ring and scribe line), IC and PD layout has to match at input pins (see fig. 9)



The pad center x/y positions are given below related to the chip origin 0/0 next to PIN 5 (see fig. 8, dimensions excl.Seal ring and scribe line (about +/-50µm), numbers in table below are to be defined later):

	Left			Bottom			Right			Top		
PIN	X/µ	Y/µ	PIN	X/µ	Y/µ	PIN	X/µ	Y/µ	PIN	X/µ	Y/µ
1			5			7			11		
2			6			8			12		
3						9			13		
4						10					

die size: 0.8 mm x 1.6 mm (goal)
bondpad window: 90µmx90µm,
minimum bondpad pitch pitch : 126µm
die thickness: 300µm
bondpad material: Aluminium,
substrate: VSS

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				Norm		
				COM FO E IC		
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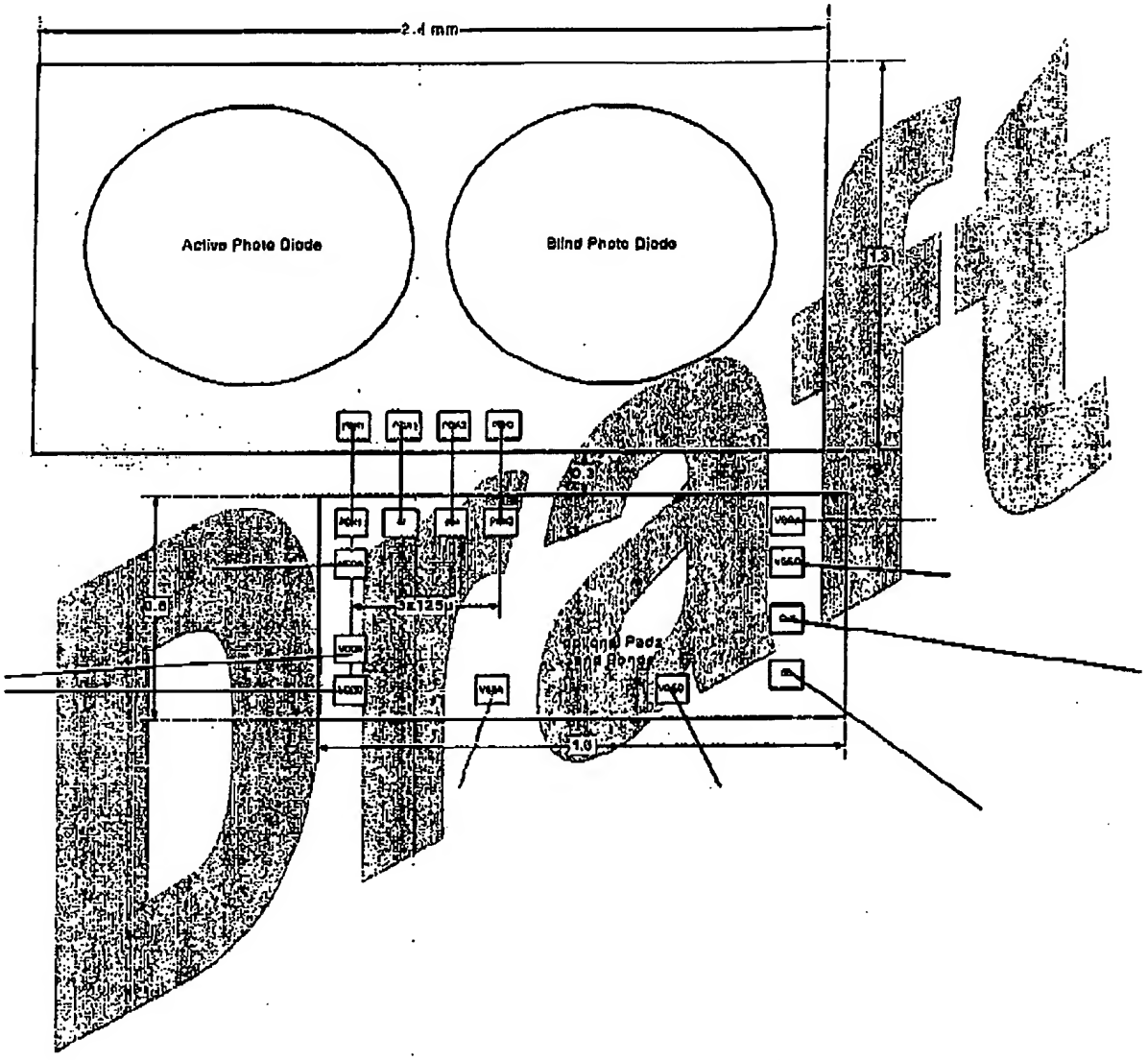
51		18 10 02	scr			Blatt 12/13
Zust.	Mitteilung	Datum	Name			

FIG. 9 : ASSEMBLY PROPOSAL FOR PHOTODIODE AND IC :



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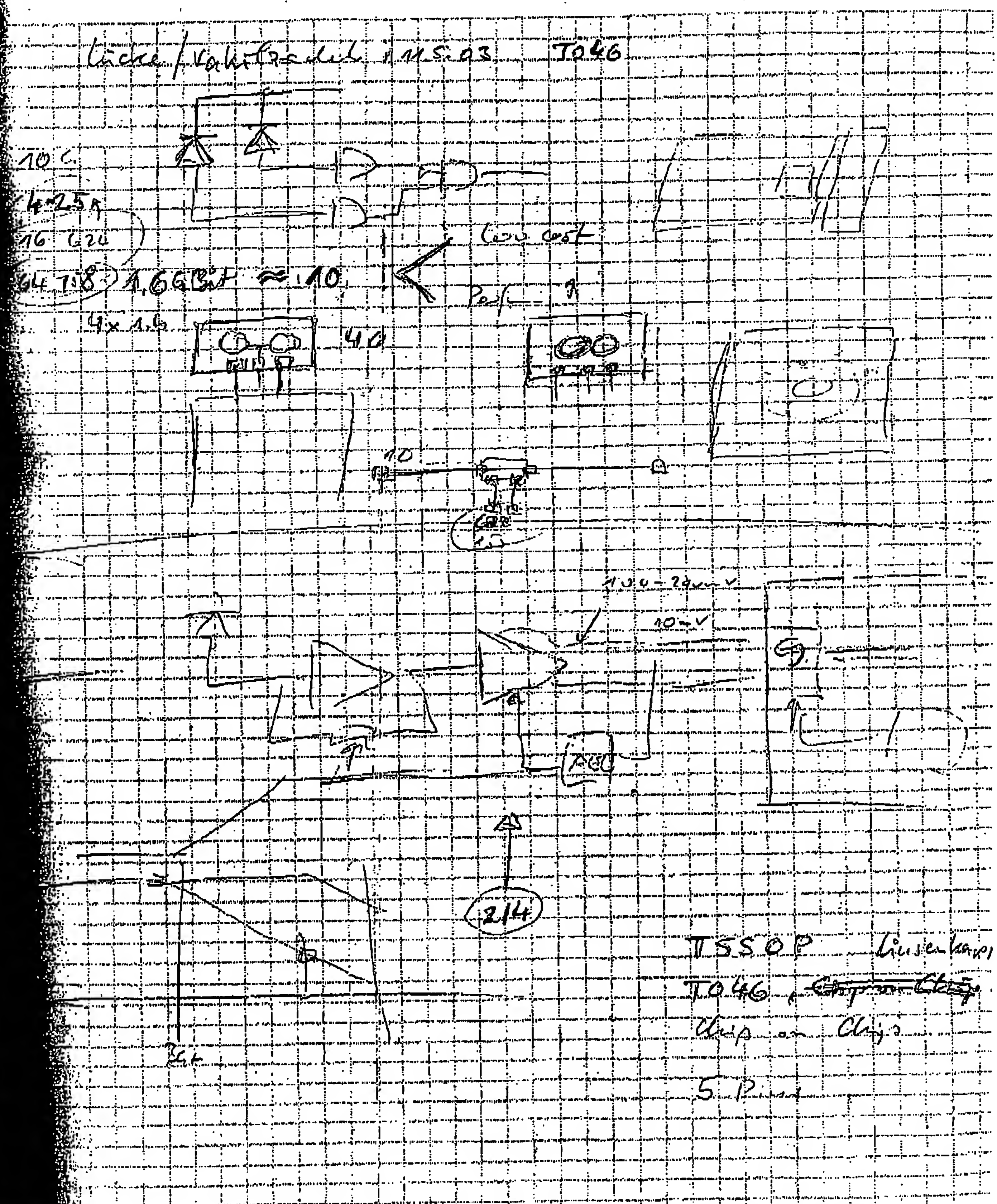
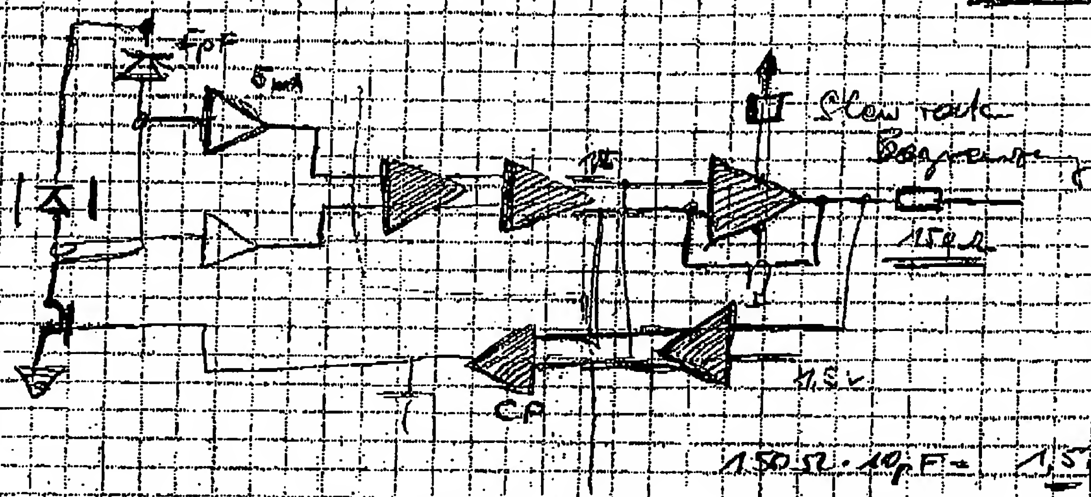

T046
low cost
1,6GBit ≈ 10
4x 1,6
40
AGC
214
TSSOP
T046
Chip on Chip

Köppe anrufen

Konzept MOST Rx → 27.9.0



$150\,\Omega \cdot 10\,pF = 1{,}5\,ns$

10 pF, 3 ns max

$I = C \frac{dU}{dt}$ $\frac{3V}{3ns} \cdot 15\,pF =$ $\frac{3}{5}$ ~~10~~ W^{-2}

6 mA 3,3 mA min

3 mA

$U = L \cdot \frac{dI}{dt}$ ~~1nH~~ $\cdot \frac{4\,mA}{3\,ns}$ 0,? mV

2 nH 4 mV

1 mV $X_{PX} = \frac{1}{j\omega C} = \frac{1}{j\, 9\,MHz\, 2\pi \cdot 10\,pF}$

~~1 kΩ~~ 318 Ω Photodioden Widerstand ≤ 50 M

$\frac{1\,mV}{318\,\Omega} = 3\,\mu A$